

FIG. 1
(PRIOR ART)

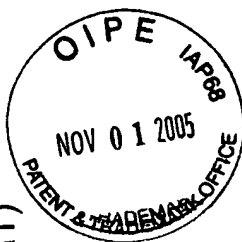
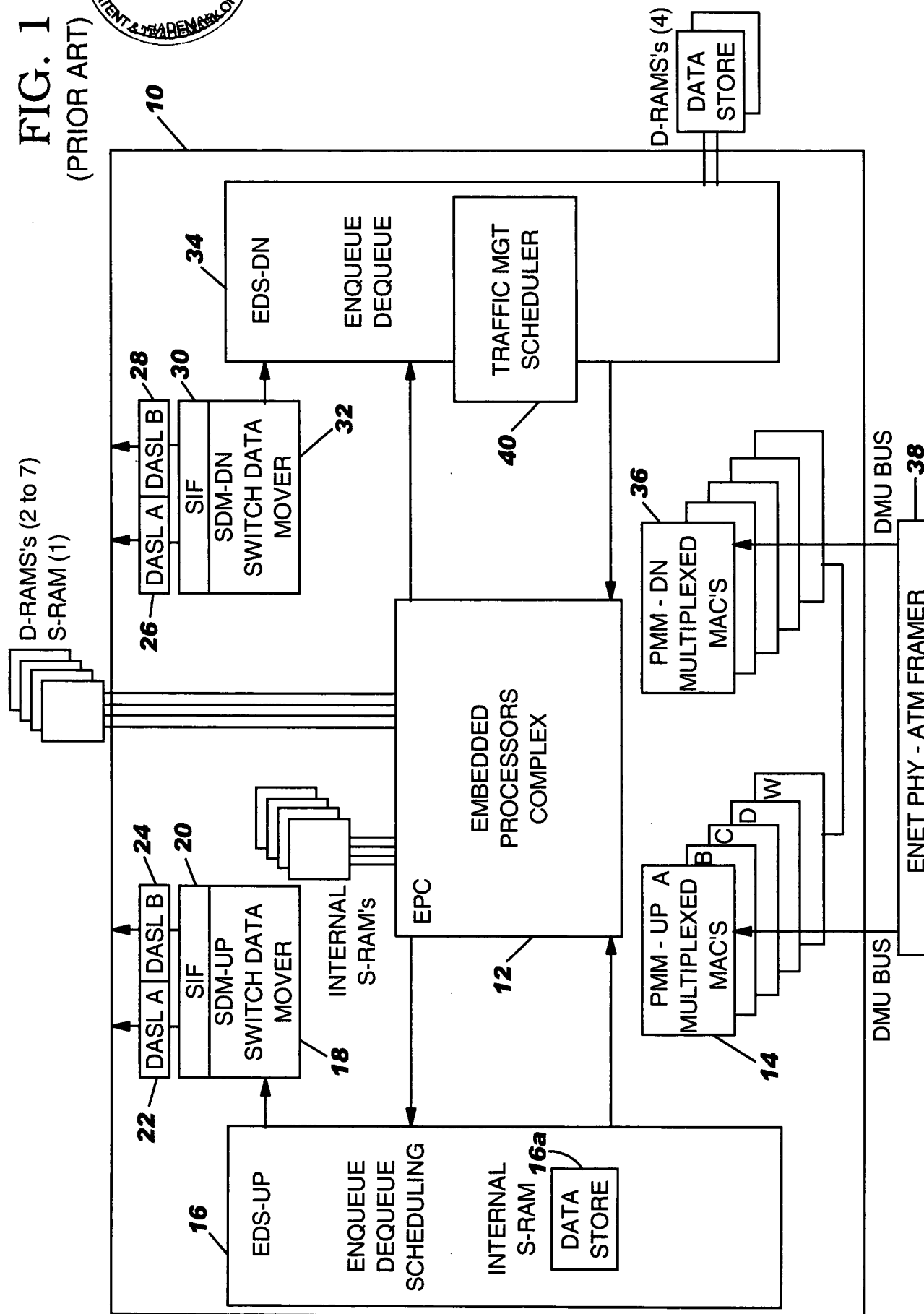


FIG. 2

(Prior Art)

BLOCK DIAGRAM OF THE EPC

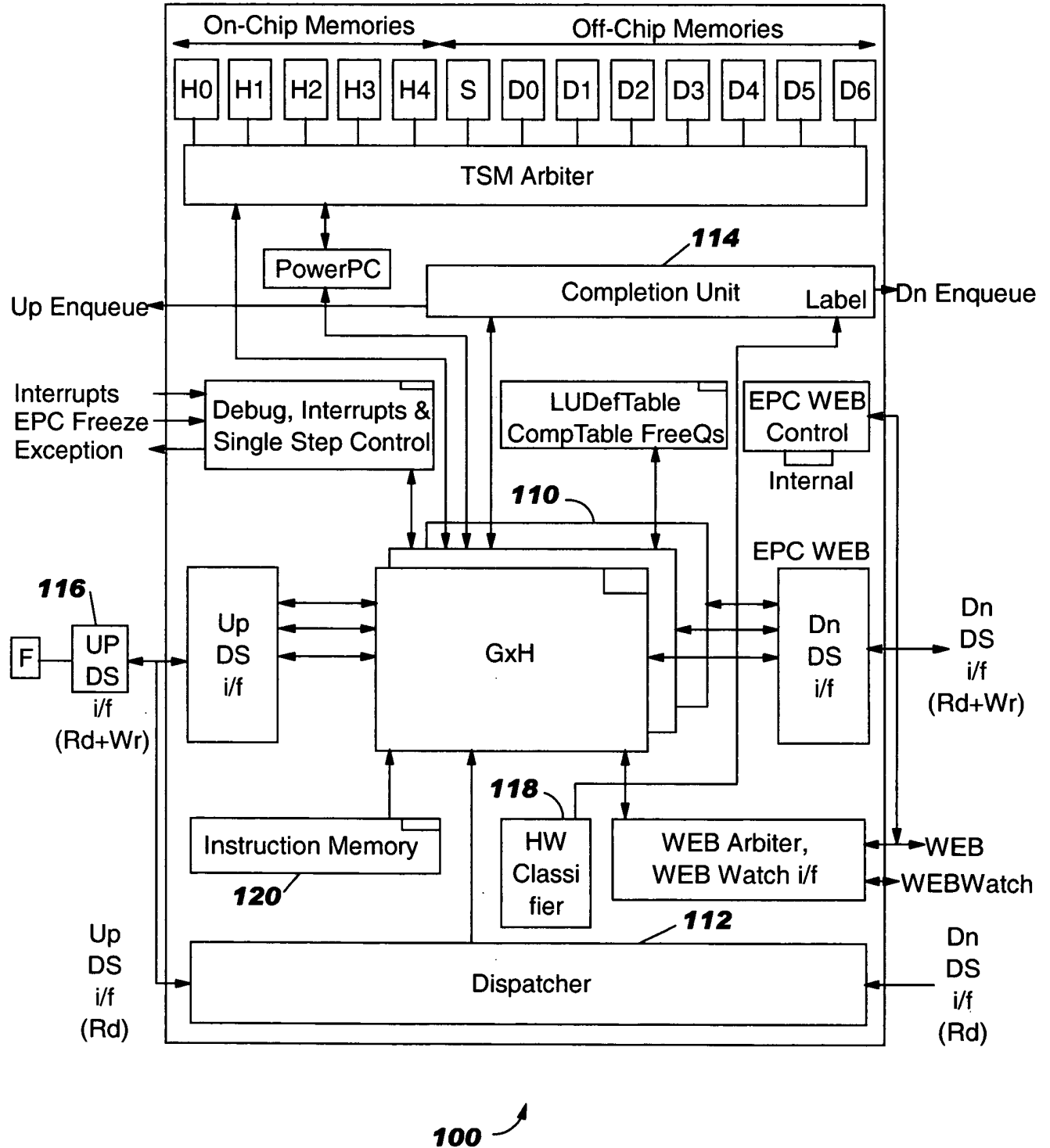


Fig. 3

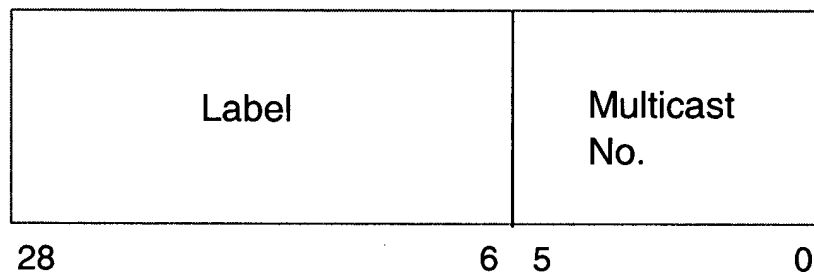


FIG. 4

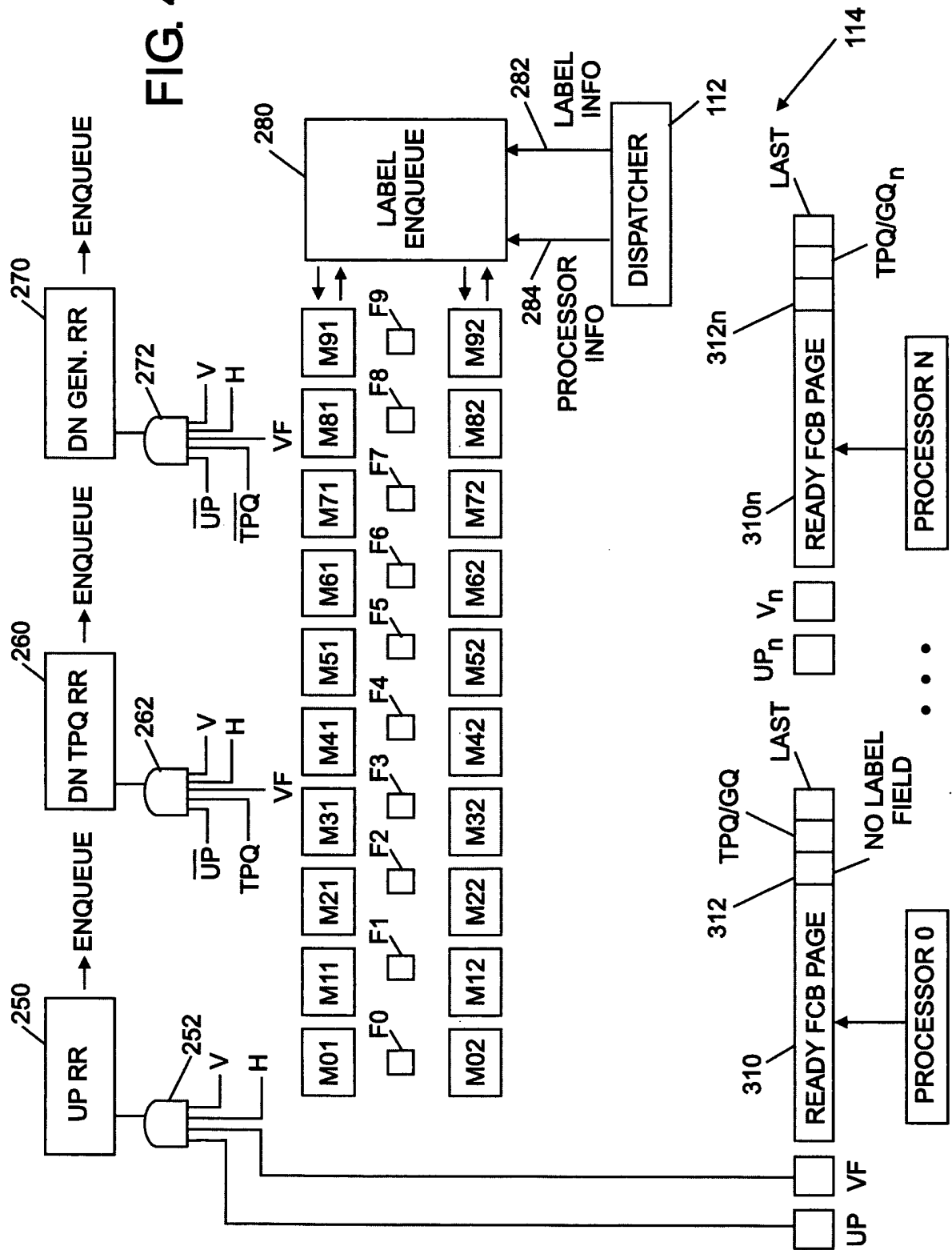
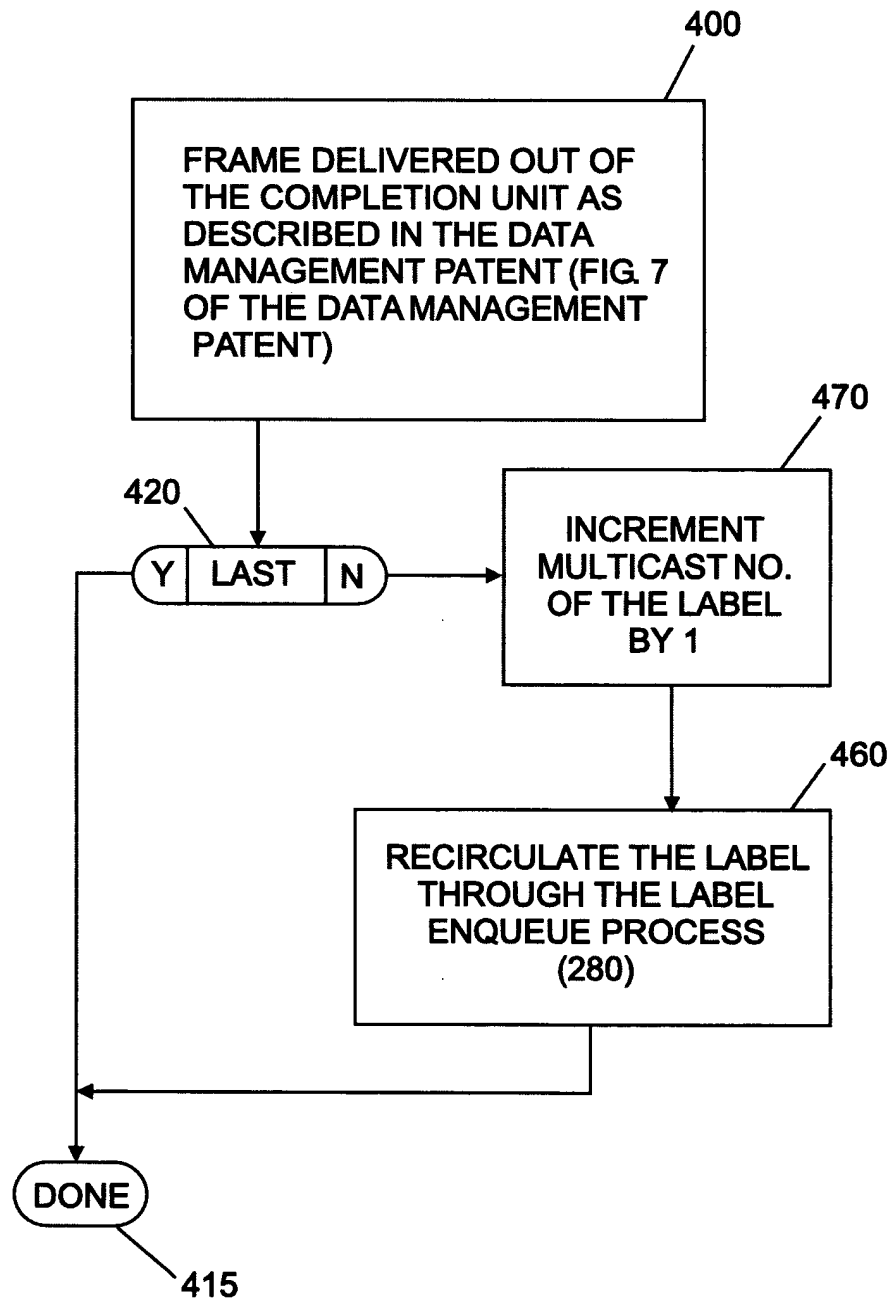


FIG. 5



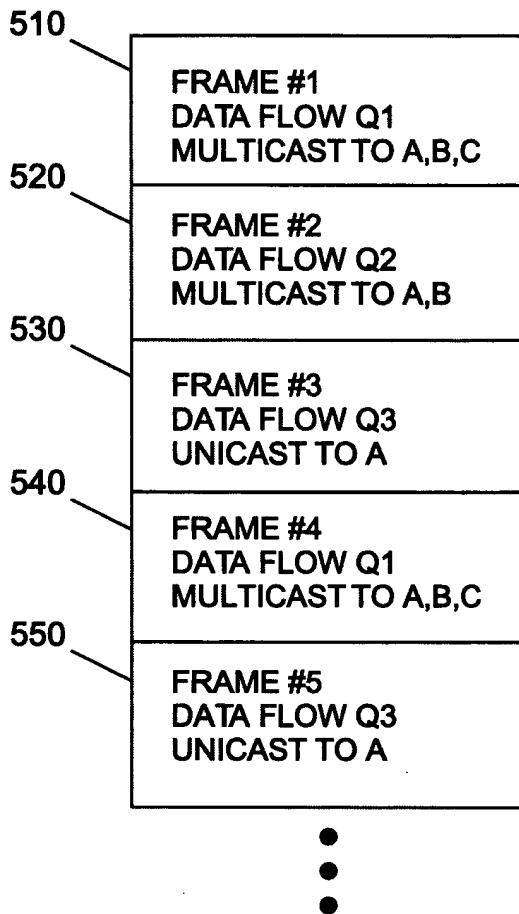


FIG. 6

FIG. 7

FRAME	PROCESSOR	LABEL	DESTINATION	
1	0	Q1+0	A	701
1	0	Q1+1	B	702
2	7	Q2+0	A	703
3	5	Q3+0	A	704
4	2	Q1+0	A	705
2	7	Q2+1	B	706
4	2	Q1+1	B	707
1	0	Q1+2	C	708
4	2	Q1+2	C	709
5	4	Q3+0	A	710